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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,079	12/23/2003	Uming Ko	TI-29632.1	8111

23494 7590 02/19/2008
TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
FULK, STEVEN J	

ART UNIT	PAPER NUMBER
2891	

NOTIFICATION DATE	DELIVERY MODE
02/19/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com
uspto@dlemail.itg.ti.com

Office Action Summary	Application No.	Applicant(s)	
	10/743,079	KO, UMING	
	Examiner	Art Unit	
	Steven J. Fulk	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *42-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *42-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Art Unit: 2891

DETAILED ACTION

Response to Appeal Brief

1. In view of the Appeal Brief filed on December 10, 2007, PROSECUTION IS HEREBY REOPENED. A new ground(s) of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the

> international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 42, 45, 48 and 51 are rejected under 35 U.S.C. 102(e) as being anticipated by Tamura '068.

Tamura discloses a semiconductor wafer comprising a plurality of integrated circuits (figs 1A & 2A; col. 1, lines 39-40; integrated circuit separated from wafer, which inherently has a plurality of circuits before separation) and a method of manufacturing thereof, wherein each of the integrated circuits is separated from the other of the integrated circuits by a scribe region (fig. 2, chip edge 204 is where dicing occurred, thus the scribe region) at the periphery of each the integrated circuit; providing a centrally disposed core region (figs. 2 & 4, "core logic") in each of the circuits; providing at least one bond pad (fig. 2, 208A) disposed between the core region and the scribe region; providing an electrostatic discharge device (210a); and providing an I/O buffer (fig. 2, I/O cell 225a; col. 1, lines 50-53, I/O cells contain I/O buffers) disposed between the scribe region and the core region and laterally of the bond pad relative to the core region and the scribe region.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 43-44, 46-47, 49-50 and 52-53 rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura '068 in view of Countryman et al. '892.

Tamura discloses all of the elements of the claim(s) as set forth in paragraph 3 above, but the reference does not explicitly disclose the electrostatic discharge device to be disposed at least partially beneath the bond pad. Countryman teaches an integrated circuit device and method of manufacturing thereof comprising the steps of: providing a semiconductor substrate (fig. 5, 32) which includes a scribe (fig. 4, chip separation boundaries are shown by metallization 20, which is inherently the scribe region) at the periphery of the substrate and a centrally disposed core region (fig. 1; col. 2, lines 35-40, circuit 10 has devices within it, considered core circuits); providing at least one bond pad (fig. 5, 20) disposed between the core region and the scribe region (fig. 1); providing a electrostatic discharge device (fig. 5, diodes 26/40, 27/41, etc) disposed at least partially beneath the bond pad; and providing an I/O buffer disposed between the scribe region and the core region (fig. 1, 22/24; col. 2, lines 35-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to disposed the electrostatic discharge device of Tamura at least partially beneath the bond pad as taught by Countryman. One would have been motivated to do this because Countryman taught that disposing the electrostatic discharge device at least partially beneath the bond pad reduces the required area for the ESD device (Countryman; col. 2, lines 4-19), thus allowing the chips to be made smaller as desired by chip designers and manufacturers (col. 2, lines 21-31). The teaching of Countryman is especially applicable to figure 4 of Tamura, where Tamura shows the EDS devices 210 occupying extra space between

the chip edge and the core logic area, wherein this space would be reduced if ESD device 210 was partially formed under bond pad 208 of fig. 2.

Response to Arguments

6. Applicant's arguments with respect to claims 42-53 have been considered but are moot in view of the new ground(s) of rejection as set forth above.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Pettersson '851, Yuan '043, Davis '183, Strauss '999 and Huang '065 disclose an integrated circuit wherein an ESD device is disposed at least partially beneath a bond pad.

Peleska '549, Sugasawara '539 and Andresen '379 disclose an ESD device and an I/O buffer disposed between a scribe region and a core circuitry region.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571)272-8323. The examiner can normally be reached on Monday through Friday, 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven J. Fulk
Patent Examiner
Art Unit 2891

February 6, 2008

/BRADLEY W BAUMEISTER/
Supervisory Patent Examiner, Art Unit 2891